REMARKS

In response to the Office Action mailed February 7, 2006, The Applicants respectfully request reconsideration. To further the prosecution of this Application, the Applicants submit the following remarks and have canceled claims. The claims as now presented are believed to be in allowable condition.

Claims 1-10 and 39-41 were pending in this Application. By this Amendment, claim 3 has been canceled and claim 1 has been amended to include the subject matter of the cancelled claim. Additionally, claim 41 has been amended to include the subject matter of claim 3. Accordingly, claims 1, 2, 4-10, and 39-41 are now pending in this Application. Claims 1 and 41 are independent claims.

Rejections under §102 and §103

Claims 1-9 and 39-41 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,866,475 (Yanagida). Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yanagida in view of U.S. Patent No. 2,933,412 (Thayer). Claims 6-8 were further rejected under 35 U.S.C. §103(a) as being unpatentable over Yanagida in view of U.S. Patent No. 5,866,475 (Lawler).

The Applicants respectfully traverse each of these rejections and request reconsideration. The claims are in allowable condition.

The Office Action has rejected independent claims 1 and 41. Taking amended claim 1 as an example, the claim relates to a circuit board processing system that comprises a circuit board fabrication stage, a solder fusing stage, and a washing stage. As recited, the circuit board fabrication stage is configured to fabricate a circuit board having a set of circuit board pads. The solder fusing stage is coupled to the circuit board fabrication stage and is configured to (i)

apply flux and solder concurrently to the set of circuit board pads, and (ii) activate the flux and melt the solder to form a set of substantially flat solder coatings which is fused to the set of circuit board pad. The solder fusing stage is also configured to print a paste onto the set of circuit board pads through a metallic stencil, the paste containing the flux and the solder. The washing stage is coupled to the solder fusing stage and is configured to remove contamination from a surface of the circuit board having the circuit board pads and from the set of substantially flat solder coatings which is fused to the set of circuit board pads.

Yanagida discloses a method for forming solder bumps (Title). In Yanagida's description of the related art, Yanagida explains that, in order to form a solder bump, an electrode pad 12 composed of an Al alloy or the like is formed on a silicon substrate 10 by a sputtering method, and then a surface protective layer 11 composed of an insulating film such as polymide film and silicon nitride film is coated on the substrate 10 (column 1, lines 41-46 and Fig. 7A). Then, an opening is formed in the surface protective layer 11, thereby to form a connecting hole for exposing the electrode pad 12, and a Ball Limiting Metal (BLM) film 14 composed of a barrier metal layer is formed with patterning on the electrode pad 12 thereafter (column 1, lines 46-50). Next, a resist film 18 is formed on the substrate, and is applied with patterning further so as to form an opening portion 16 where the BLM film 14 is exposed (column 1, lines 51-54 and Fig. 7B). Next, a solder film 20 is formed on the substrate by vapor deposition or the like (column 1, lines 55-56 and Fig. 7C). In succession, the resist film 18 is removed by resist peeling and cleaning, and the solder film 20 on the resist film 18 is lifted off at the same time (column 1, lines 56-59). As a result, the solder film 20 remains behind only in the opening portion 16 (column 1, lines 59-61 and Figs. 7B and 7D). Next, the solder film 20 is dissolved by heat treatment, and the solder film 20 located on the BLM film 14 is transformed into ball-shaped solder, thus forming a solder ball bump 22 (column 1, lines 62-65 and Fig. 7E).

Independent claims 1 and 41 were rejected under 35 U.S.C. §102(b) as being anticipated by Yanagida. However, Yanagida does not teach or disclose all of the elements of the Applicants' amended claims 1 and 41 and as such, claims 1 and 41 patentably distinguish over Yanagida.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

In the Office Action response of December 12, 2005, the Applicants asserted that claim 1 patentably distinguished over Yanagida because Yanagida does not disclose a circuit board processing system having a solder fusing stage which is configured to activate flux and melt solder to form a set of substantially flat solder coatings which is fused to a set of circuit board pads, as recited in claim 1.

In response to this argument, the Office Action recites on page 4, that the Examiner agrees with the Applicants arguments. However, the Office Action further states that "this, however, does not mean that Yanagida does not meet the claimed limitation."

On page 4, the Office Action recites that:

> The examiner understands that, as with any other claim limitation, functional language is acceptable so long as it sets definite boundaries on the patent protection being sought. In re Barr, 170 USPQ 33 (CCPA 1971). A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is

> capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See In re Casey, 152 USPQ 235 (CCPA 1967) and In re Otto, 136 USPQ 458, 459 (CCPA 1963). To put it another way: While the features of an apparatus may be recited either structurally or functionally, claims directed to an apparatus must be distinguished from the prior art in terms of structure rather than function. In the instant case, just as in applicant's invention, Yanagida teaches heating stage to form the solder structure (col. 1, ll. 45-67). It is the examiner's position that the Yanagida's heating stage would be capable of performing in the claimed manner. When the examiner has reason to believe that functional language asserted to be critical for establishing novelty in claimed subject matter may, in fact be a characteristic of the prior art, the burden of proof is shifted to the applicant to prove that the subject matter shown in the prior art does not possess the characteristic relied upon. *In re Fitzgerald et al.* 205 USPQ 594.

Applicants understand In re Barr, In re Otto, In re Casey, and In re Fitzgerald but respectfully submit that the Office Action has misapplied these cases to the claims as currently amended. In particular, claim 1, as amended with claim 3, now recites the solder fusing stage as being "configured to print a paste onto the set of circuit board pads through a metallic stencil". There is no metallic stencil taught in Yanagida as required for a proper rejection under 102(b) (see *Verdegaal Bros. v. Union Oil Co. of California* and *Richardson v. Suzuki Motor Co.*). Furthermore, it is unclear how one could modify Yanagida to print paste onto the set of circuit board pads through a metallic stencil. In particular, Yanagida deals with packaging a semiconductor device on mounting substrate (e.g., see column 1, lines 5-10 of Yanagida), not mounting a circuit board package on a circuit board.

In the Response to Arguments section, the Office Action cites In re Casey which held that if the prior art structure is capable of performing the intended use, then it meets the claim. The Office Action then contends that "Yanagida teaches heating stage to form the solder structure (col. 1, ll. 45-67). It is the examiner's

position that the Yanigida's heating stage would be capable of performing in the claimed manner" (page 4 last paragraph of the Office Action). In re Casey is incorrectly applied particularly since there is no mention whatsoever that, in Yanagida, the heating stage is capable of printing a paste onto a set of circuit board pads through a metallic stencil as recited in claim 1. As mentioned above, Yanagida does not mention any metallic stencil whatsoever. Instead Yanagida discloses the use of a resist film procedure to form solder bumps. Yanagida does not teach or suggest a solder fusing stage configured to print a paste onto the set of circuit board pads through a metallic stencil as claimed by the Applicants.

The Office Action further cites In re Otto which held that in a claim drawn to process of making, the intended use must result in manipulative difference as compared to the prior art. In re Otto has also been misapplied particularly since there is clearly a manipulative difference includes in the Applicants independent claims, i.e., the printing of paste through a metallic stencil.

The Office Action further cites In re Fitzgerald which held that the PTO "can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his [or her] claimed product. . . . Whether the rejection is based on 'inherency' under 35 U.S.C. 102, on '*prima facie* obviousness' under 35 U.S.C. 103, jointly or alternatively, the burden of proof is the same." However, for the burden to shift to the applicant, the Office Action must first present evidence or reasoning tending to show inherency (see MPEP 2114, 2173.05(g) and 2181). In particular, as recited in MPEP chapter 2112, section IV:

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy,* 17

> USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original)

The Applicants assert that the Patent Office has not met the criteria for relying on the theory of inherency in its rejection. Instead, the Office Action has stated that

> [i]n the instant case, just as in applicant's invention, Yanagida teaches heating stage to form the solder structure (col. 1, ll. 45-67). It is the examiner's position that the Yanagida's heating stage would be capable of performing in the claimed manner.

The Office Action further stated that "the examiner has reason to believe that functional language asserted to be critical for establishing novelty in claimed subject matter may, in fact be a characteristic of the prior art" (see page 5, lines 1-3 of the Office Action).

The Applicants are unclear how such recitations meets the requirement to "provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." In particular, with respect to claim 1, there is no evidence or reasoning indicating why the Yanagida heating stage inherently uses a metallic stencil. Moreover, the Applicants respectfully submit that there is no inherency since Yanagida deals with packaging a semiconductor device on mounting substrate not mounting a circuit board package on a circuit board.

Because Yanagida does not teach or suggest a solder fusing stage configured to print a paste onto the set of circuit board pads through a metallic stencil as claimed by the Applicants and because the Office Action has not shown that the metallic stencil, as claimed, inherently flows from Yanagida under the theory of inherency, claims 1 and 41 patentably distinguish over the cited prior art, and the rejection of claims 1 and 41 under 35 U.S.C. §102(b) should be

withdrawn. For the reasons stated above, independent claims 1 and 41 patentably distinguish over the cited prior art, and the rejection of the independent claims under 35 U.S.C. §102(b) should be withdrawn. Accordingly, claims 1 and 41 are in allowable condition. Additionally, claims 2, 4-10, and 39-40 which depend from claim 1 should also be allowed for at least the reasons presented above.

Dependent claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Yanagida in view of Thayer. Claims 6-8 were further rejected under 35 U.S.C. §103(a) as being unpatentable over Yanagida in view of Lawler. However, because these claims depend from allowable independent claim, the rejection is moot.

Also, if the Office Action is indeed asserting the theory of inherency as the reason for maintaining the rejection, the *Applicants respectfully request withdrawal of the finality of the rejection as being improper*. As a reminder, under MPEP Chapter 706.07(a):

> second or any subsequent actions on the merits shall be final, *except where the examiner introduces a new ground of rejection that is neither necessitated by applicant's amendment of the claims nor based on information submitted in an information disclosure statement* filed during the period set forth in 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p). (Emphasis added)

The Applicants contend that the assertion of the theory of inherency to maintain the rejection of claims 1-9 constitutes a new ground of rejection that was neither necessitated by the Applicant's amendment nor based on information submitted in an information disclosure statement. Reconsideration of the finality of the present Office Action is respectfully requested.

Conclusion

In view of the foregoing remarks, this Application should be in condition for allowance. A Notice to this affect is respectfully requested. If the Examiner believes, after this Response, that the Application is not in condition for allowance, the Examiner is respectfully requested to call the Applicants' Representative at the number below.

The Applicants hereby petitions for any extension of time which is required to maintain the pendency of this case. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 50-3661.

If the enclosed papers or fees are considered incomplete, the Patent Office is respectfully requested to contact the undersigned collect at (508) 616-2900, in Westborough, Massachusetts.

Respectfully submitted,

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